Homework #13

1) Full adder from class : adding 2 2-bit numbers

$$\begin{array}{r} C_2\, C_1 \\ X_1\, X_0 \\ Y_1\, Y_0 \\ \hline C_2\, Z_1\, Z_0 \end{array}$$

C_2, carry bit

Truth table

	C_1	X_1	Y_1	C_2	Z_1
	0	0	0	0	0
*	0	0	1	0	1
*	0	1	0	0	1
	0	1	1	1	0
*	1	0	0	0	1
	1	0	1	1	0
	1	1	0	1	0
*	1	1	1	1	1

For Z_1 true : make Boolean statement for the starred rows

$$Z_1 = \bar{C}_1(\underbrace{\bar{X}_1 Y_1 + X_1 \bar{Y}_1}_{X_1 \oplus Y_1}) + C_1(\bar{X}_1 \bar{Y}_1 + X_1 Y_1)$$

$$= \bar{C}_1(X_1 \oplus Y_1) + C_1(\bar{X}_1 \bar{Y}_1 + X_1 Y_1)$$

$A + 0 = A$

2nd term: $\bar{X}_1\bar{Y}_1 + X_1Y_1 = \bar{X}_1\bar{Y}_1 + X_1Y_1 + \overbrace{X_1\bar{X}_1}^{0} + \overbrace{Y_1\bar{Y}_1}^{0}$

$= (X_1 + \bar{Y}_1)(\bar{X}_1 + Y_1)$

↓ dem.

$= \overline{(\bar{X}_1 Y_1)} \cdot \overline{(X_1\bar{Y}_1)}$

↓ dem

$= \overline{\bar{X}_1 Y_1 + X_1\bar{Y}_1}$

$= \overline{X_1 \oplus Y_1}$

$\Rightarrow \quad z_1 = \bar{C}_1(X_1 \oplus Y_1) + C_1\overline{(X_1 \oplus Y_1)}$

$U \equiv X_1 \oplus Y_1$

$\Rightarrow \quad z_1 = \bar{C}_1 U + C_1\bar{U}$

$z_1 = C_1 \oplus U$

$\Rightarrow \quad \boxed{z_1 = C_1 \oplus (X_1 \oplus Y_1)}$ as required.

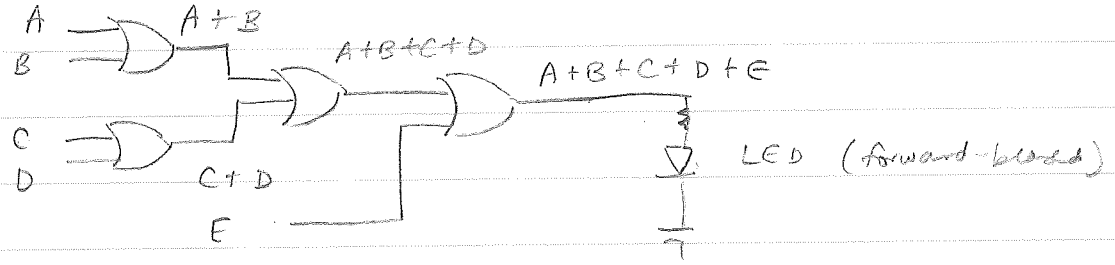
8.6) Want alarm system to light an LED when any of 5 doors are open

Open door → high

Assume LED turns on when high voltage level across it

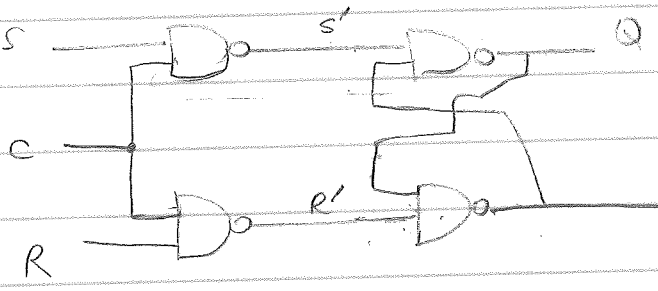
Use only 2-input logic gates

Want: $A+B+C+D+E = Q$



8.7) Make a clocked flip-flop w/ functionality as

Eggleston Fig 8.31



NAND:

0 0	1
0 1	1
1 0	1
1 1	0

NAND output goes high if either input low

Q low ⇒ $\bar{Q}$ high

$\bar{Q}$ low ⇒ Q high

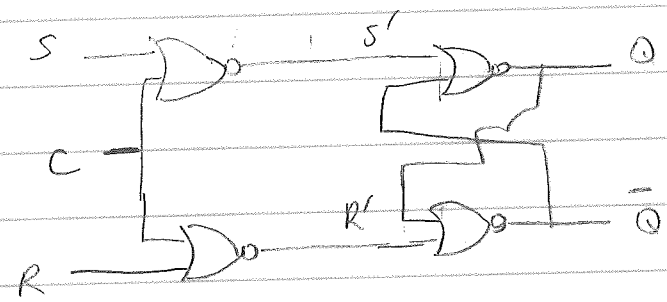
Behavior of basic flip flop on the right

S'	R'	Q	$\bar{Q}$	
0	0	1	1	→ avoid, unstable
0	1	1	0	
1	0	0	1	
1	1	no change		{ if Q=0, $\bar{Q}$=1 / if $\bar{Q}$=0, Q=1 } (bistable)

Now behavior with S, C, R added on the left: if C is low S' and R' are both high, and there is no change at Q, $\bar{Q}$. If C is high, S and R are inverted

Replacing NAND's with NOR's:

		S'	R'	Q $\bar{Q}$
With C high	S R			
	0 0	1	1	no change
	0 1	1	0	0 1
	1 0	0	1	1 0
	1 1	0	0	unstable



NOR

0 0	1
0 1	0
1 0	0
1 1	0

NOR output goes low if either input high

So as for the NAND gate FF,

Q high ⇒ $\bar{Q}$ low

$\bar{Q}$ high ⇒ Q low

Also bistable

So we have for the right hand FF

S'	R'	Q	$\bar{Q}$
0	0	no change	
0	1	1	0
1	0	0	1
1	1	0	0 → a word, unstable

Now adding S, C, R on the left:

If C is high, S' and R' go low,

so no change at the output

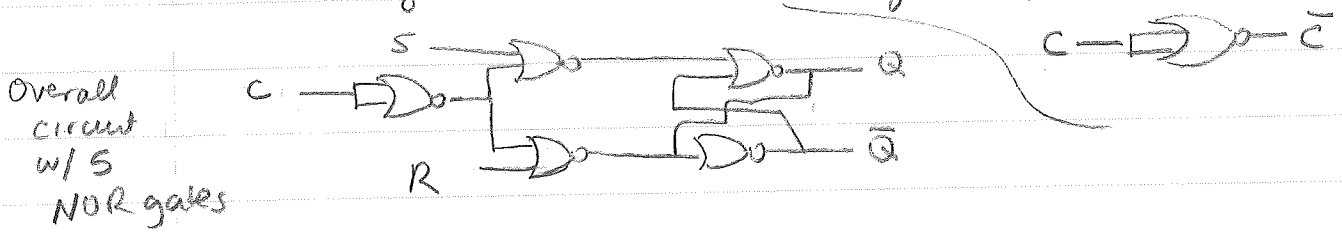
If C is low,

S	R	S'	R'	Q	$\bar{Q}$
0	0	1	1	unstable	
0	1	1	0	0	1
1	0	0	1	1	0
1	1	0	0	no change	

So we get the same behavior as the version with NANDs for $(S, R) \to (Q, \bar{Q})$

(different unstable condition)

To get the same behavior for C, use an inverter



Overall circuit w/ S NOR gates