Duke University
Department of Physics

Physics 271 Spring Term 2017

PRACTICE (FINAL) MIDTERM SOLUTIONS

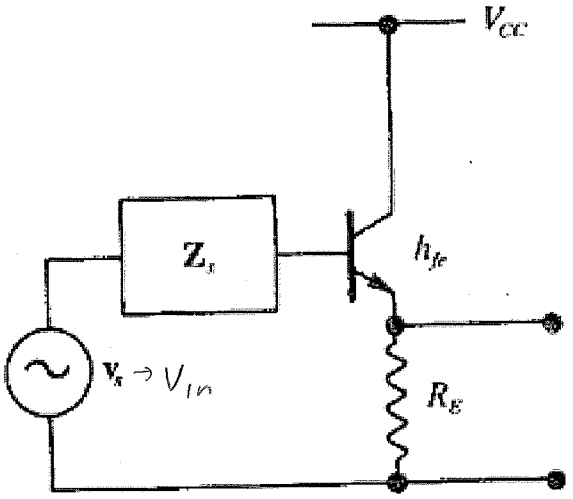
I will abide by the Duke Community Standard. Name: _____

This is a closed book exam, with two sides of one page cheat sheet allowed. Calculators are allowed, but only for basic calculations: you may not use special memory, graphing etc. functions. You must always show your work for credit; all answers must be justified. **You must hand in your cheat sheet with your test.**

Problem 1: (10 points)

Derive an expression for the output impedance of the simplified CC circuit shown in terms of given quantities. Assume that the transistor works without DC bias resistors. Neglect all hybrid parameters except h_{fe}, but do not assume $h_{fe}R_E >> |\mathbf{Z}_s|$.

↓ β ↳ β



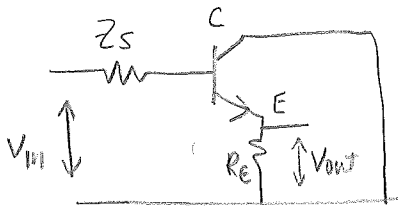
$$Z_{out} = \frac{V_{out}(R_L \rightarrow \infty)}{i_{out}(R_L \rightarrow 0)}$$

Note: $i_1 = i_1(R_L \rightarrow \infty)$, $i_b = i_b(R_L \rightarrow \infty)$ not same as currents when output shorted

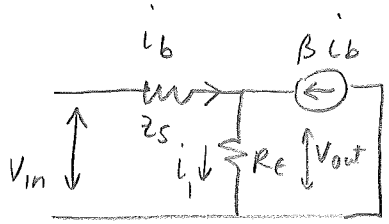
This is a common collector amp (emitter follower)

AC equivalent:

$V_{CC} \rightarrow$ gnd



replace with transistor model →



With output open: $i_1 = i_b + \beta i_b$

For: $R_L \rightarrow \infty$ $\quad V_{out} = R_E i_1 (R_L \rightarrow \infty)$

$V_{out} = R_E i_b (1+\beta)$

Voltage drops to gnd $\quad V_{in} = Z_s i_b + R_E i_1 = Z_s i_b + R_E(1+\beta) i_b$

$$V_{out}(open) = \frac{R_E i_b (1+\beta)}{Z_s i_b + R_E(1+\beta) i_b}(V_{in}) = \frac{R_E(1+\beta)}{Z_s + R_E(1+\beta)} V_{in}$$

Now with output shorted : $\quad i_{b(short)} = \frac{V_{in}}{Z_s} =$

Through short $\quad i_1(short) = i_{b(short)} + \beta i_{b(short)}$

$$\Rightarrow \quad i_1(\text{short}) = (1+\beta)\, i_b(\text{short}) = (1+\beta)\frac{V_{in}}{Z_s}$$

$$\Rightarrow \quad Z_{out} = \frac{V_{out}(\text{open})}{i_1(\text{short})}$$

$$= \frac{R_E(1+\beta)}{Z_s + R_E(1+\beta)} \; V_{in} \; \frac{1}{(1+\beta)V_{in}/Z_s}$$

$$Z_{out} = \frac{R_E Z_s}{Z_s + R_E(1+\beta)}$$

For the assumption given $\beta R_E \gg Z_s$,

$$Z_{out} \sim \frac{R_E Z_s}{R_E(1+\beta)} \sim \underline{\underline{\frac{Z_s}{1+\beta}}}$$

For $Z_s \gg \beta R_E$, (the assumption I should have used)

$$Z_{out} \sim \frac{R_E Z_s}{Z_s} = R_E$$

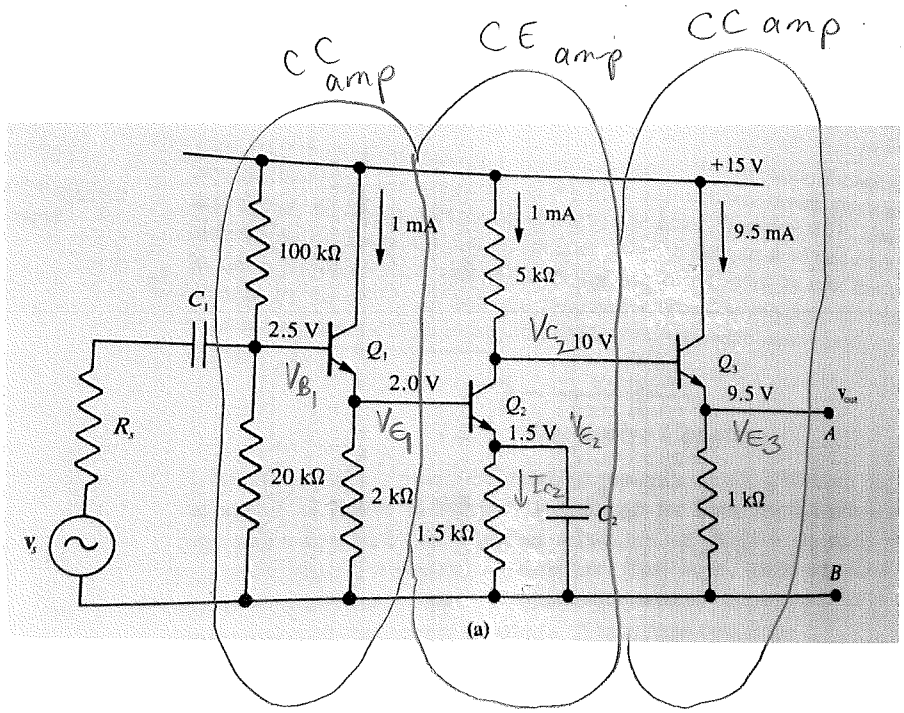
(actually the answer in Eggleston Table 4.2, but it's really only valid for small R_E)

Problem 2 (15 points)

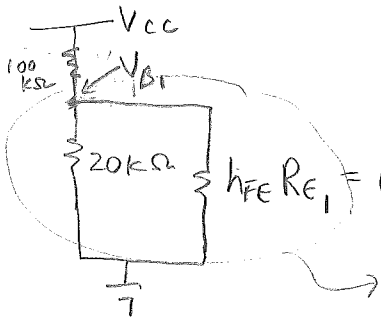
Consider the given circuit.

a. Identify the different "components" of the multi-transistor circuit.

b. The DC quiescent voltages of the figure all assume h_{FE} is very large. Work out the voltages exactly if $h_{FE} = 50$ and $V_{PN} = 0.5$ V.



First DC stage



$h_{FE} R_{E_1} = (50)(2) = 100\,k\Omega$

$R_{eq} = \frac{20 \cdot 100}{120} = 16.67\,k\Omega$

$V_{B_1} = \left(\frac{16.67}{100 + 16.67}\right) V_{CC} = 2.14\,V$ ($V_{CC} = 15\,V$)

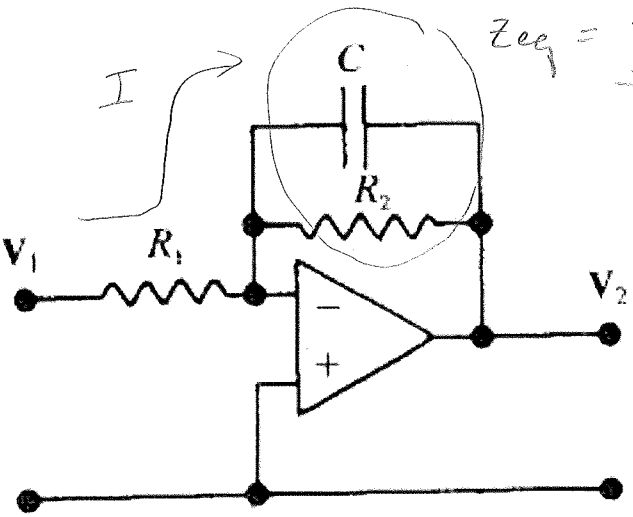
$V_{E_1} = (2.14 - 0.5)V = 1.64\,V = V_{B_2} \Rightarrow V_{E_2} = 1.64 - 0.5 = 1.14\,V$

$I_{C_2} = (1.14\,V)/(1.5\,k\Omega) = 0.76\,mA \Rightarrow V_{C_2} = 15\,V - (0.76)(5) = 11.2\,V$

$V_{E3} = V_{B_3} - 0.5\,V = V_{C_2} - 0.5V = 10.7\,V$

Problem 3 (15 points)

Assuming an ideal op-amp, determine $\mathbf{G}(j\omega)$ for the circuit shown. Sketch the approximation to $|\mathbf{G}|$, labeling magnitudes, corners and slopes.



$$Z_{eq} = \frac{\frac{1}{jwC} \cdot R_2}{1/jwC + R_2} = \frac{R_2}{1 + R_2 C j\omega}$$

$$G(j\omega) = \frac{V_2}{V_1}$$

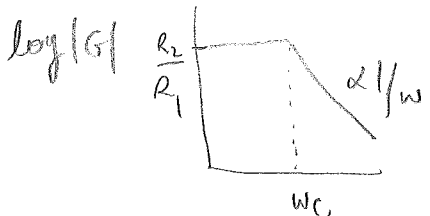
$$\frac{V_1 - 0}{R_1} = \frac{0 - V_2}{Z_{eq}}$$

$$\frac{V_2}{V_1} = -\frac{Z_{eq}}{R_1} = -\frac{R_2}{R_1}\left(\frac{1}{1 + jwR_2C}\right) \quad \text{(inverting)}$$

For w small, $|G| \sim R_2/R_1$

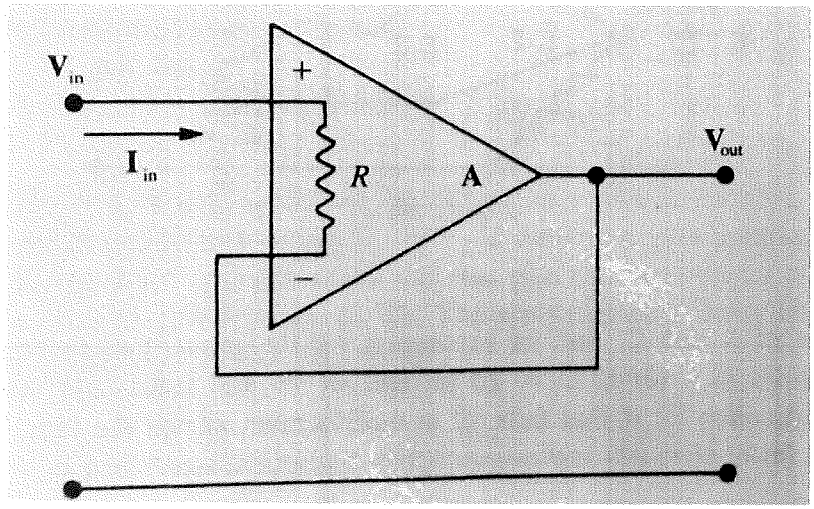
w large, $|G| \sim \frac{1}{R_1 w C}$

corner for $\frac{R_2}{R_1} = \frac{1}{R_1 w C} \Rightarrow w = 1/R_2 C$



Problem 4 (10 points)

Find the input impedance of the circuit shown in terms of the open-loop gain **A**.



$$Z_{in} = \frac{V_{in}}{I_{in}}$$

$$I_{in} = \frac{V_{in} - V_{out}}{R}$$

$V_{out} = A(V_{in} - V_{out})$ → open loop gain

$$V_{out}(1+A) = A V_{in}$$

$$V_{out} = \left(\frac{A}{A+1}\right) V_{in}$$

$$I_{in} = \frac{V_{in} - \frac{A}{A+1} V_{in}}{R} = \left(1 - \frac{A}{A+1}\right)\frac{V_{in}}{R} = \frac{1}{A+1}\frac{V_{in}}{R}$$

$$\Rightarrow Z_{in} = \frac{V_{in}}{I_{in}} = \underline{\underline{(A+1)R}}$$

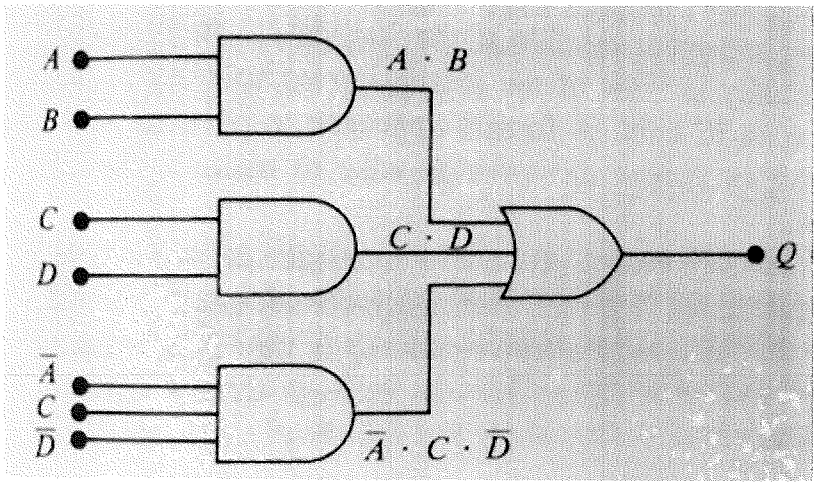
Problem 5 (8 points)

Explain the term "signal race" and describe a common general method of avoiding it in a circuit.

A "signal race" is a situation in a logic circuit in which logic-level transitions do not occur at well-defined times, so that output can be unpredictable. Signal races can result in "glitches" – short, unwanted and unstable transitions. The standard solution is to design digital circuits to have synchronous transitions, that all occur at the time of a standard clock pulse input.

Problem 6 (12 points)

If the input to the given circuit is written as a number $ABCD$, write the nine numbers that will yield a true Q, in binary, decimal and hexadecimal.



$Q = A \cdot B + C \cdot D + \overline{A} \cdot C \cdot \overline{D}$

	A	B	C	D	A · B	C · D	$\overline{A}$ · C · $\overline{D}$	Q
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	1	0	1
4	0	1	0	0	0	0	0	0
5	0	1	0	1	0	0	0	0
6	0	1	1	0	0	0	1	1
7	0	1	1	1	0	1	0	1
8	1	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	0
10	1	0	1	0	0	0	0	0
11	1	0	1	1	0	1	0	1
12	1	1	0	0	1	0	0	1
13	1	1	0	1	1	0	0	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	1	0	1

Inputs making Q true

Hex | Decimal | Binary

Problem 7 (15 points)

Consider the following logical function: $F = (A + \overline{B})C + B\overline{C}$.

a. Make a truth table for the three inputs A, B, C that implements this function.

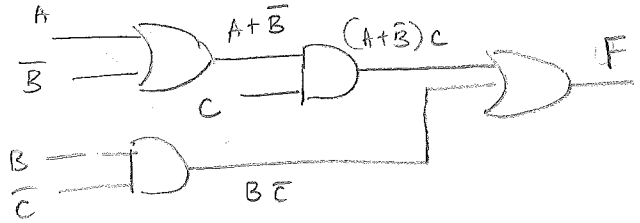
b. Draw a circuit diagram using logic gates that implements the logic. Do not manipulate the expression mathematically— implement the function exactly as written. You may assume you have both signals and inverted signals available as inputs. Label the output of each logic gate with its value.

c. Now implement the above function with no more than three 2-input gates which are from the set (NOR, NAND, AND, OR, XOR). Use Boolean algebra to reduce the expression. Once again label each gate output.

a)

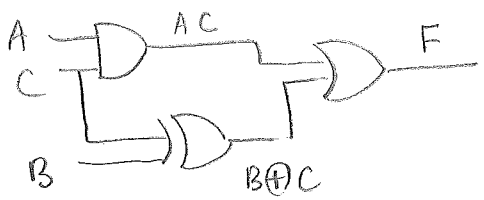
A	B	C	$A+\overline{B}$	$(A+\overline{B})C$	$B\overline{C}$	F
0	0	0	1	0	0	0
0	0	1	1	1	0	1
0	1	0	0	0	1	1
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	0	1	1	1	0	1
1	1	0	1	0	1	1
1	1	1	1	1	0	1

b)



c) $Q = (A+\overline{B})C + B\overline{C} = AC + \overline{B}C + B\overline{C}$

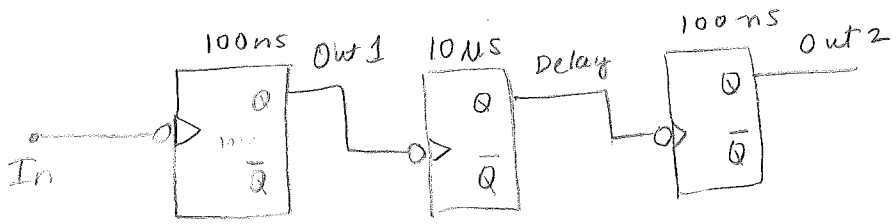
$\overline{B}C + B\overline{C} = B \oplus C$

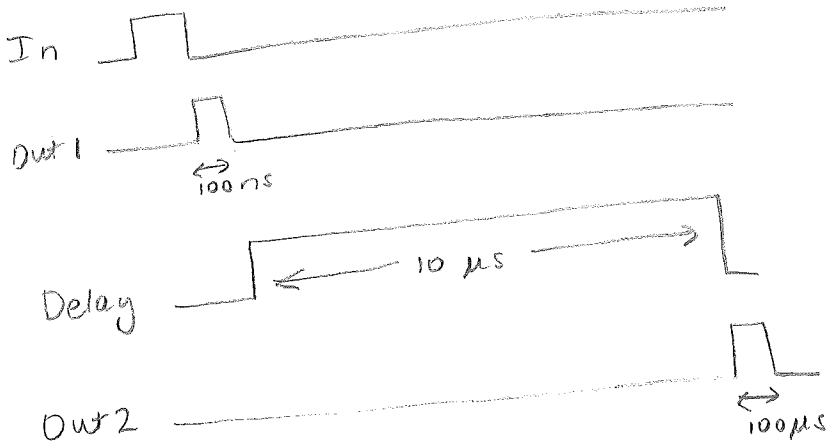


Problem 8 (15 points)

Design a circuit to create two 100-ns pulses 10 microseconds apart.

Use "one-shot" flip-flops





(not to scale)

This could also be implemented using a counter