Duke University
Department of Physics

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WUN2K FOR LECTURE 24

These are notes summarizing the main concepts you need to understand and be able to apply.

- A *latch* stores the state of an input data line on its output according to the value on a control line.
  - For a "ones catching" latch, the output Q follows the input D so long as the control input C is false. If C becomes true, Q latches true as soon as D is true, and doesn't return to false until both Q and D are false.
  - For a "D-type" or "transparent" latch, Q follows D so long as C is true, and freezes the output at Q when C goes false.

- A *flip-flop* is a bistable device, for which the outputs $Q\bar{Q}$ can be either 01 or 10. For an RS (reset-set) flip-flop, which can be implemented with NOR gates, an RS input of 00 causes no change on the output. An RS input of 10 ("reset") sets Q to 0 (and $\bar{Q}$ to 1); an RS input of 01("set") sets Q to 1 (and $\bar{Q}$ to 0). An input $RS = 11$ is to be avoided as it can lead to an undefined condition when the input changes to 00.

- *Clocked flip-flops* change their state at their $Q\bar{Q}$ outputs according to the state of their clock input. These may be "static", if they are sensitive to just the logic level at the clock input, or "dynamic" if they are *edge-triggered*. Edge-triggered flip-flops change state at the output at the time of a logic transition at the clock input. "Active high" flip-flops are triggered when the clock pulse goes from $0 \rightarrow 1$; "active low" flip-flops are triggered when the clock pulse goes from $1 \rightarrow 0$. The symbol for an edge-triggered clock input is a small rightward-pointing triangle, with a circle for active low. Such flip-flops may also have set

and reset inputs which serve to initialize the output, regardless of the inputs.

- A common flip-flop which is often used with edge triggering is the *JK flip-flop*, which has two inputs, J and K as well as a clock input. When $JK = 00$, the output $Q\bar{Q}$ does not change at the clock pulse. When $JK = 01$ or 10, $Q\bar{Q}$ is set to 01 or 10 respectively at the clock trigger time. When $JK = 11$, the output *toggles* when a clock pulse comes in: it changes from 01 to 10 or 10 to 01.

- Arrays of flip-flops arranged in parallel can be used as *registers* to store bits. A *shift register* has the ouput of each flip-flop connected to the input of the next, so that bits in parallel can be read out serially with each clock pulse.