Duke University
Department of Physics

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WUN2K FOR LECTURE 22

These are notes summarizing the main concepts you need to understand and be able to apply.

- Logic gates can be combined to produce any kind of logical operation. A general method for designing circuits to implement a given operation is:

  1. Write the truth table corresponding to the desired operation.
  2. Translate the table into Boolean algebra (writing either rows corresponding to Q true conditions, or Q false conditions).
  3. Reduce the Boolean statement as far as possible; De Morgan's theorem is often useful.
  4. Implement the Boolean statement as logic gates.

- The *exclusive OR (XOR)* logic operation gives $Q = A \oplus B$ true when either A or B (but not both) are true. This operation can be implemented using a combination of basic logic gates.

- Real circuits take finite time to make the transition between logic levels. A *timing diagram* (logic levels as a function of time at places of interest) can be helpful for analyzing circuit behavior.

  – A pathology of *asynchronous* digital circuits is the *signal race*, which can result in a timing *glitch* when levels do not change exactly simultaneously due to propagation and transition delays. A standard fix is to make circuits *synchronous*, so that logic levels change only in step with a regular clock pulse.

- *Logic families:* digital logic is implemented with different conventions for 0 and 1, according to internal designs. Various conventions exist, and typically standard IC chips are available from multiple manufacturers for a given logic family. Here are some popular ones:

  - *TTL: Transistor-to-Transistor*: this is the most "standard" logic family and makes use of bipolar transistors. Packages come in different flavors for high-speed or low-power use. Logic 1 corresponds to $\sim$+5 V and logic 0 corresponds to $\sim$0 V. Typical gate delay speeds are $\sim$15 ns.
  - *CMOS: Complementary Metal Oxide Semiconductor (CMOS)*: CMOS devices are low power usage but can be slow ($\sim$ 70 ns gate delays). Logic 1 corresponds to $3 - 18$ V and logic 0 corresponds to 0 V. This employs MOSFET technology, and devices can be very sensitive to static.
  - *ECL: Emitter-Coupled Logic*: this family provides high-speed transitions (gate delays better than 10 ns) but uses a lot of power. Logic 1 corresponds to ~ -0.8 V and logic 0 corresponds to -1.5 V. Input and output are usually differential, which decreases sensitivity to noise.
  - *NIM: Nuclear Instrumentation Module:* this family is used mostly in nuclear and particle physics (usually in the context of "modules"). Logic 1 corresponds to -0.8 V and logic 0 corresponds to ~ 0 V. Transitions are fast, $\sim$ns.

- Modern electronics circuits often make use of *Application Specific Integrated Circuits (ASICs).* These are packaged chip devices designed for specific uses, using "gate arrays" with connections that can be configured according to desired functionality at manufacture time. *Field Programmable Gate Arrays (FPGAs)* are even more flexible: digital circuits can be designed in software, and connections between gates can be configured and reconfigured "on the fly" to modify the functionality. These are widely used for prototyping ASICs, or used themselves in circuits.