# FREQUENTLY ASKED QUESTIONS

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## Content Questions

### What again is the practical application difference between a FET and transistors we've studied previously?

FETs tend have larger input impedance than bipolar transistors, and the gate of a FET typically draws much less current than the base of a bipolar transistor. So if you have an application that needs lots of transistors and you don't want to draw too much current from the input, you might want to use FETs. FET transistor parameters are also less sensitive to temperature and the response is more linear. But they are also more sensitive to static. In practice, there are many considerations for circuit design (including cost).

### Why do we choose the operating point from the $I_d$ vs $V_{gs}$ plot instead of the $I_d$ vs $V_{ds}$ characteristic (similar to what we did with the bipolar transistor?) Can we use $I_d$ vs $V_{ds}$ instead?

Yes, you can use the $I_d$ vs $V_{ds}$ plot to find the operating point. You can use the right-hand part of the circuit Kirchoff Loop equation to write $I_d = \frac{V_{dd}-V_{ds}}{R_s+R_d}$, draw it as a load line and find the intersection with the graph like Eggleston Fig. 5.10. This will give you $I_d$ for a given $V_{gs}$ in the saturation regime. You would then find $V_g$ for this $I_d$ and $V_{gs}$, from $I_d = \frac{V_g-V_{gs}}{R_s}$, and choose resistors for that $V_g$ from the voltage divider equation for the left hand side of the circuit.

### Why can you assume $r_{\text{out}}$ is infinite?

This is really only a good approximation in the saturation regime for a FET. $r_{\text{out}}$ is effectively the reciprocal of the slope of the $I_d$ vs $V_{ds}$ curve. In the saturation regime, the curve is very flat (no more current for more applied $V_{ds}$), with a slope near zero, and the output resistance is very large.

**Where does each of the FET equations apply? (saturation vs. linear regime)**

- The saturation voltage is given by $V_{ds(\text{sat})} = V_{gs} - V_t$, where $V_t$ is the threshold voltage for turn-on of current $I_d$. This is independent of regime; it specifies the saturation voltage.
- In the linear regime where $V_{ds} < V_{ds(\text{sat})}$, $I_d = K(2V_{ds(\text{sat})} - V_{ds})V_{ds}$, where $K$ is a constant.
- In the saturation regime where $V_{ds} > V_{ds(\text{sat})}$, we have $I_d = KV^2_{ds(\text{sat})}$.

**Can $g_m$ be solved for? Or do we need to know $i_d/v_{gs}$ in the saturation regime?**

Well, $g_m$ is a *property of the FET*– it will be specified by the FET manufacturer. So if you have to design a circuit for a particular FET, this will be a fixed parameter.

Now if you have flexibility in designing a circuit, you might want to choose a FET with a particular $g_m$ (although note that it can vary from FET to FET of a particular type) to make an amplifier with particular properties.

**Why is it $v_{\text{in}} = v_{gs} + g_m v_{gs} R_s$ and not $v_{\text{in}} = v_{gs} - g_m v_{\text{gs}} R_s$ for the common source amplifier?**

It's the relative signs that matter here. For $v_{\text{in}}$ positive, $G$ is more positive than $S$. Take $i_1 = g_m v_{gs}$ as the current circulating counterclockwise in the right-hand loop (up through $R'_L$, left across the current-source, down through $R_s$ to ground).

If you start with $v_{\text{in}}$ on the left-hand side, a Kirchoff loop gives $v_{\text{in}} - v_{gs} - i_1 R_s = 0$, so $v_{\text{in}} = v_{gs} + g_m v_{gs} R_S$.

**Why use so many modes of transistor when they all do similar things?**

Well, they do similar things, but not exactly the same things, and have different properties. The choice depends on your application need. You might have certain impedance requirements, or current requirements, or switching speed requirements, or sensitivity to temperature, or stability requirements, or whatever. Cost can also be a factor.