FREQUENTLY ASKED QUESTIONS

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Content Questions

What makes it possible for FETs to control current with voltage directly, but that bipolar transistors need to use current for control?

Well, it's not that bipolar transistors *need* to use current to control the current from collector to emitter; we just often to think of their use in that way (we *could* think of the voltage from base to emitter, or from collector to emitter, as a control, since I_c does depend on both of those).

But the nature of the devices differ so that what we usually think of as a control quantity differs. For the bipolar transistor case, there is some current from the base into the device, and which I_c vs V_{ce} curve you are on depends on I_b— so the I_c saturation current depends on I_b. So we tend to think of I_b as the quantity that we vary to get a desired I_c. Physically, the story is a bit complicated— current flowing into the base means electrons pulled out of the base, which prevents the base from charging up and blocking collector-emitter current flow.

For the FET case, there is very little current into the transistor from the gate. For the JFET case, that's because the junction is reverse-biased; for MOSFETs, it's because the gate is actually insulated from the channel. I_g is just tiny and not so relevant. In the FET case, the value of V_{gs} is what determines which I_d vs V_{ds} curve you are on, and hence is what determines the saturation current (or channel resistance, in the resistive regime). So we tend to think of V_{gs} as the control parameter. Physically, we can think of this bias voltage as creating an electric field that determines how easy it is for current to flow in the channel (that's the "field effect").

Why is the current flowing into the FET gate so small?

Inside an operating JFET, the gate is always reverse-biased with respect to the channel, i.e., there's always a depletion zone next to the gate. Very little current flows in through the gate; the main current is flowing from drain to source. For MOSFETs, there's actually an insulator between the gate and

the channel, so very very little current gets through from the gate into the FET.

What are the relative sizes of the p-regions and n-regions in FETs?

It depends on the specific kind of FET, and the configurations can vary quite a bit. I think in general the doped regions around the gate are smaller than the channel.

For JFETs, drain and source look the same. Can we reverse drain and source in the experimental setup?

In principle, yes. In practice, it may depend on the specific device design— I believe some JFETs can be used symmetrically, but others may be engineered asymmetrically.

Do all of the FETs have the same $I_d - V_{gs}$ slope? Or are the curves just similar?

They are not exactly the same, but they tend to have similar shapes.

What is the meaning of "pinch-off region"?

The "pinch-off region" (or "saturation region") refers to operation of a FET with V_{ds} more than a few volts. Look at Figs. 5.2 and 5.10 in Eggleston. In this regime, the current I_d is almost independent of V_{ds} (for a given V_{gs}). What's happening inside the transistor is that the depletion regions due to the biases have enlarged to allow only a narrow path for the current (hence the "pinch-off" nomenclature). In this regime, as V_{ds} increases, it increases the length of the depletion zone, which increases the resistance, basically compensating for increased current due to increased voltage— so the current remains nearly constant. The particular constant value depends on V_{gs}, which sets the width of the depletion zone. This is the normal operating regime of a FET, in which current going through depends on the control gate-to-source voltage V_{gs}.

(You can also have a complete pinch-off when the bias voltage is so large that the entire channel is non-conductive and you get basically no current.)

Do p-channel FETs mirror the n-channel $I_d - V_{gs}$ graphs?

P-channel FETS will have the n-type and p-type semiconductor regions reversed with respect to n-channel, so the V_{gs} bias will be opposite for the same operation (current still flows from the drain to the source). Yes, the I_d vs V_{gs} curve will be the mirror image, with increasing I_d going up to the left.

How do we use the linear regime? What exactly are we calculating when we draw the curve $I_d = f(V_{ds})$?

Well, the I_d vs V_{ds} curve is a *property of the FET*, for a given V_{gs}, and it's some function $I_d = f(V_{ds})$ (with a linear turn-on and then a saturation). For each value of V_{gs} there's a different curve. In today's example, we were trying to figure out what V_{gs} value to use to make a FET switch (like in Eggleston Fig. 5.9) turn on (i.e., pull a large I_d) or turn off.

To figure that out, we use Ohm's Law to write $I_d = \frac{V_{dd}-V_{ds}}{R_d}$. That's a straight line with y-intercept V_{dd}/R_d and x-intercept V_{dd} on the I_d vs V_{ds} plot. For a given $V_{gs} = V_g$ (where V_g is the input voltage), the intersection of this line and the corresponding I_d vs V_{ds} curve tells us the value of I_d you get for V_g at the input.

So, let's take the JFET example (see Fig. 5.10). When we want the switch on (large I_d), the intersection of the line and top curve gives a large I_d. So $V_{gs} = 0$ will turn the switch on. For switch off, we want small I_d, so we'd pick the bottom curve with $V_{gs} = -5\ V$ (or thereabouts) where the intersection gives small I_d.

Note that the other kinds of FETs give different ranges of V_{gs} corresponding to the different I_d vs V_{gs} curves. So if we are using different kinds of FETs, different input voltages will turn the FET on and off.

What is the functional difference between bipolar transistors and FETs in electronics applications?

In our simplified models, here is how we treat these different devices functionally:

- A bipolar transistor in its operating regime (with V_{ce} greater than about 2 V) has $V_{be} = V_{pn}$ and the current from collector to emitter is given by the Transistor Man equation, $I_c = \beta I_b$ (with AC-equivalent expression $i_c = \beta i_b$). We tend to think of the collector current as being controlled

by the base current. (For V_{ce} less than about 2 V, the I_c behavior is nonlinear.)

- A JFET in its operating regime draws approximately zero (∼pA) current at the gate. In its operating ("pinch-off") regime, where V_{ds} is greater than about 2 V, we tend to think of the drain-to-source current as being controlled by the gate-to-source voltage. (For V_{ds} less than about 2 V, the JFET acts like a variable, but linear, resistor, with resistance controlled by V_{gs}.)

How are FETs and bipolar transistors applied differently? What is the technical advantage of using one kind over the other?

For some applications, you could use either. FETs however are rather more "modern" and have a number of advantages: they have larger input impedance (drawing very little current), better temperature characteristics, better performance at high frequency, better linearity at low bias voltage. MOSFETs in particular are used almost exclusively in large-scale integrated circuits because they use much less power.

Bipolars tend to be quite robust and are less sensitive to static than FETs (especially MOSFETs).

How important is it for us to know about bipolar transistors?

Although bipolar transistors aren't as commonly used as FETs these days, they do still have uses. It's a good idea to have the basic concepts about how both kinds work.

What quantitatively is relevant to FETs?

This is a broad question— but FET behavior can be quantitatively described by model equations (here for JFETs):

- The saturation voltage is given by $V_{ds(\mathrm{sat})} = V_{gs} - V_t$, where V_t is the threshold voltage for turn-on of current I_d.
- In the linear region where $V_{ds} < V_{ds(\mathrm{sat})}$, $I_d = K(2V_{ds(\mathrm{sat})} - V_{ds})V_{ds}$, where K is a constant.
- In the saturation region where $V_{ds} > V_{ds(\mathrm{sat})}$, we have $I_d = KV_{ds(\mathrm{sat})}^2$.