# FREQUENTLY ASKED QUESTIONS

March 2, 2017

## Content Questions

### What exactly is the idea behind the charge clamp?

The idea of the diode clamp is that you can enforce a DC offset with a diode. If you are driving a signal through a capacitor, then you could have a DC offset according to how much charge was on the capacitor when it was first connected to the supply (total voltage at $V_0$ is $V_s + V_{\text{cap}}$, where $V_{\text{cap}} = Q/C$). This could be some unpredictable value, and might be undesirable. To get a specific offset, you can put a diode across the output. The diode would only conduct when $V_0$ on the right hand side of the capacitor is negative. When $V_0$ is positive, current can't flow through the diode and charge is trapped on the capacitor (positive charge on the right hand side). With positive voltage on the right hand side, the diode never conducts and the charge on the capacitor can never swing negative. So what you end up with is a DC offset at the output. (BTW you could change the offset by putting a reference voltage, e.g. DC power supply, in the branch with the diode.)

### How effective are the best regulators?

How bad the ripple is on the output will typically depend on the input— quality of regulation is often given as a fraction of the input variation. An ordinary kind of regulator would give an output that has a variation a few percent of the input voltage variation. I am not sure what the absolute best ones could do, but googling around I found some that give $\sim$0.02%. (The performance can be temperature dependent.)

There are other criteria in choosing a regulator— things like the current that can be provided, power consumption, temperature stability, *etc.* may drive the choice more than output stability.

### How do they make transistors so small?

Making semiconductor electronic components is a whole subfield of engineering... sophisticated methods have been developed over the past several decades for creating vast arrays of microscopic doped devices on chips. The fact that semiconductors exist in the solid state at room temperature, and are stable, is very helpful for making them into tiny, robust devices.

### Why aren't pnp transistors used as often?

One of the main reasons that npn transistors are more popular than pnp is that conductivity tends to be higher in n-type materials (the majority charge carriers are electrons). For npn, the transistor parameters tend to be better (more on these later).

Also, npn transistors may be easier to manufacture: see this link.

### Why does the base need to be biased as well?

For normal transistor operation, there needs to be forward bias from the base to the emitter (in the direction of the pn "diode")— in fact this is critical for operation of the transistor. This bias makes the emitter less positive, counteracting the effect of the diffusion-created depletion region (in fact the depletion region can completely go away). Electrons from the emitter are then able to drift towards the collector (attracted by the positive voltage on the collector side), creating the current $I_C \sim I_E$ (which is in the direction of positive charge flow, so opposite to the direction of travel of the electrons).

### What's the difference between the collector and the emitter?

In normal transistor operation, the emitter is where the electrons spill over from into the base, and they cruise across to the collector (so in fact the positive current goes from collector to emitter across the transistor).

In our simplified npn sandwich picture of a transistor, the situation looks symmetric, and looks as if the difference between collector and emitter depends only on the applied bias: base to emitter corresponds to the forward-biased side and base to collector (or emitter to collector) corresponds to the reverse-biased side. However for real-life transistors, it *does* matter which terminal is which— they are designed for the current to flow in a particular direction. (The arrangement of semiconductors inside a transistor doesn't necessarily look like the conceptual sandwich diagram— design of these things is a whole subfield of engineering well beyond the scope of this course!)

**For the biased npn transistor, why is only the electron energy in the collector region changed, and nothing happens to the emitter and base regions?**

Well this is a simplified picture, and it may not have been clear in the whiteboard sketches...indeed there may be change in all the regions, but the key thing is that the bias reduces the electron energy in the collector region with respect to the emitter. That makes it easier for an electron to "fall" from emitter to collector through the base (which corresponds to current from collector to emitter).

**What determines the static forward transfer current fraction?**

I do not know exactly, but I suspect it is determined by multiple properties of the transistor: semiconductor properties, amount and type of doping, and transistor geometry.

**I'm curious about choosing different geometries for npn layouts?**

The geometries may be quite unlike our simplified sandwich picture. The n pieces are not always identical – they may have different kinds of doping and maybe even different semiconductors. Since npn transistors are normally operated with the base-emitter junction forward-biased, the construction may be optimized to handle forward current. The emitter may be more heavily doped in order to easily provide electron charge carriers, and the geometry may be devised so that there is a high efficiency for electrons to make it to the collector. Semiconductor designers can do many clever things to optimize devices for particular requirements (high current, fast switching, low noise, ease of fitting inside an integrated circuit, or whatever is important for a particular application). The details of this are beyond what we'll discuss in this course, but here is a bit more info on some particular bipolar transistor types: https://en.wikipedia.org/wiki/Bipolar_junction_transistor.

**What did the $I_C$ vs $V_{CE}$ chart tell us about changing input current?**

This plot has different curves corresponding to different values of $I_B$, the current into the base. Each curve has a roughly-constant-$I_C$ plateau corresponding to the "linear active region" where the transistor is biased and has a $V_{CE}$ above a certain value. In this region, the plateau $I_C$ value is linearly dependent on $I_B$. So we can *control* what $I_C$ is by choosing $I_B$.

**What is the significance of the linear active region?**

This "plateau" region of the bipolar transistor $I_C$ vs $V_{CE}$ curve corresponds to "normal" operation. The base-emitter pn junction is forward biased. There's a different curve for different values of $I_B$, the current into the base, with $I_C$ value in the plateau typically linearly dependent on $I_B$ with a large constant of proportionality, $I_C = \beta I_B$, where $\beta$ is something like $\sim$100. We can think of the plateau $I_C$ value in the linear active region as being controlled by the $I_B$ value.