Scalable Experimental Network of Excitable Boolean Nodes

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Context and Motivations



A neural network in the brain



A social network of college students

- Ubiquity of Large and Complex Networks

• Biology, Social, Finance, Electric Grids, Transports

- Intensive Theoretical and Analytical Studies of Real Networks

- Stability, Control, Synchronization. M.E.J. Newman, Oxford University Press (2010)
- Difficulties to Build Experimentally Large Networks
 - State of the art: 7-nodes time-delay network with lasers

Nixon et al. PRL (2011)

Excitable Nodes

- Why Excitable Nodes?

J.D. Murray, ''Mathematical Biology'', Springer (1993) A. Mikhailov, ''Foundations of Synergetics'', Springer (1994)

- Quick Recall on Excitable Dynamics



Logic Gate as Network Node

- Previous Research

- Periodic and chaotic oscillator with logic gates
 - R. Zhang et al. PRE Rapid (2009) H. Cavalcante et al. Philo. Trans. Royal Soc. A (2009)

AUTONOMOUS (a.k.a ASYNCHRONOUS) SYSTEMS : NO CLOCK!





- Major Challenges to Build Large Networks of Excitable Nodes
 - Scalability and Flexibility: rewire quickly a very large network is hard
 - Excitability: no template for a boolean version of excitable node

Experimental Platform (1)

- The Field Programmable Gate Array (FPGA) by the Numbers



- Number of available logic elements/blocks: 115,000
- Time to build/rewire a network: few minutes !
 - To be compared to months with other approaches...
- (Very) low cost : **\$300**

Altera FPGA Cyclone IV

- Principles of Implementation

- Use of hardware description language (VHDL, Verilog)
- Logic elements are wired physically on the board
 - User specifies logic function of each node and the links (network topology)
- All the features of a true experimental platform
 - Electronic noise and **heterogeneity** for nodes and links

Experimental Platform (2)

- Exploiting FPGA's Logic Elements to Build Boolean Nodes
 - Two fundamental building blocks for boolean network: **Nodes** and **Links**
 - Usable elements on the FPGA: Logic Elements with Look-Up Tables





- Building an Excitable Boolean Node on the FPGA
 - Two interconnected blocks composed of **unclocked** logic elements



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Experiment with a Single Node

- Implementation on the FPGA Board
 - Use of 40 logic elements per node
 - Logic elements are **unclocked**
 - Pulse Block: 4 elements Refractory Block: 36 elements
- Experimental Test of a Single Node
 - Pulse of width w=2.5 ns and refractory period $t_{ref} = 10$ ns (approx)



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Experiment on Small Network

- Implementation of a Small Network on the FPGA Board
 - Links use 160 logic elements and present **heterogeneity** in delays
- Approximate Zero-Lag Synchronization (ZLS)
 - \bullet Network synchronization if appropriate values of delays and t_{ref}
 - Heterogeneities (up to 2.5%) prevent perfect ZLS



Experiment on Large Network (1)

I. Kanter et al. Euro. Phys.. Lett. (2011)

- Clustered Zero-Lag Synchronization in Neural Circuits
 - Activity Mode of the entire Network governed by a **nonlocal quantity**
 - The greatest common divisor (GCD) of the directed loops
 - In theory, purely excitable systems with no noise with uniform delayed connections



GCD(A,B,C,D) = 2 => Two clusters expected

Experiment on Large Network (2)



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Conclusion

- We found an efficient way to create an excitable system with logic elements
- We implemented it on an FPGA
- FPGA: Flexible platform with great potential for studying large autonomous boolean networks
- We experiment on large network (2-3X size of the experimental state-of-art)
- Observation of approximate zero-lag synchronized clusters
- We also built a very large ring network (500 nodes)